

	DAY 1 Tuesday November 10th	DAY 2 Wednesday November 11th	DAY 3 Thursday November 12th	DAY 4 Friday November 13th	
9:00 AM	 edge lab LIVE   electronica  = Hands-On Workshop				
9:30 AM	edge lab LIVE! Keynote From Makers to Millions: Scaling Innovation for the AI Era	Edge AI Day Keynote  MICROCHIP  HAILO	CRA Day Keynote State of the CRA for Embedded-Powered Products	 Zephyr® Meetup PROGRAM TBA	
10:00 AM	 ARDUINO  SECO  congatec  Toradex Employment. Careers.	Bringing Amazon Sidewalk to Life  AVNET™  amazon sidewalk 	Cyber Resilience Act: From Compliance to Competitive Advantage  		
10:30 AM	Voice to Action: Building Portable Edge AI Applications with Linux and Containers with Raul Muñoz	Build, Sense, and Visualize featuring the Infineon PSOC™ Edge  AVNET™  	Locking down the Edge: How NVIDIA and OEMs Use TPM 2.0 to Secure Physical AI and Meet EU CRA requirements		
11:00 AM	 Qualcomm 		From Unauthenticated Netboot to CRA-Ready Industrial Gateways: Measured Boot and Remote Attestation on Baremetal RISC-V		
11:30 AM	Accelerate Embedded Development with the FRDM Automotive Platform  	Edge AI Motion Tracker on Hubble Network  	From Firmware Build to CRA Evidence: A Reproducible SBOM and Vulnerability Workflow	 yocto· PROJECT Meetup PROGRAM TBA	
12:00 PM			AI at the Edge with i.MX Applications Processors  		CRA Conformance and Raspberry Pi: A Collaborative Analysis of Compliance Dos and Don'ts 
12:30 PM					How to Be a Secure Component in the Embedded Product Supply Chain   YGREKY 
1:00 PM	Build Professional UIs with LVGL on STM32U5 Board with Gábor Kiss-Vámosi	Reinforcement Learning for Robotics with Shawn Hymel   	Patch at Scale: What CRA-Ready Software Updates Look Like in the Real World		 edge lab - LIVE -
1:30 PM			Yocto, Containers and Edge AI: Making All the Pieces Work Together		
2:00 PM	 LVGL 	Edge AI Panel Session To Be Announced	Edge Security for Cellular IoT Devices: How to Ensure Edge Security and CRA for Cellular IoT Devices with Exein and Deutsche Telekom with Thomas Roos  exein  		
2:30 PM	Managing Resource Constraints at the Embedded Edge with FPGAs with Adam Taylor  ADIUVO 			Where Should the AI Run? Making the MCU, NPU, or Cloud Decision  exein  	
3:00 PM	What If Edge Servers Were Composable? CXL, COM-HPC and CAPE	An Evening of Edge AI with Shawn Hymel 	CRA Industry Nightcap & Expert Panel: From Requirements to Evidence Across the Embedded Supply Chain 		
3:30 PM				SMARC Carrier Board Design: What Really Matters with Martin Unverdorben  SGE STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES  TRIA AN AVNET COMPANY 	
4:00 PM	I · O · T — S · T · A · R · S			 electronica INFO@EDGE LABLIVE.COM	
4:30 PM					
5:00 PM					
5:30 PM					
6:00 PM					



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|---------------------------------|-----------------------------|--------------------------------|--------------------------------|-------------------------------|
| 1. OPEN / C5.100/1 | 9. 3M / C5.100/9 | 17. Arduino (HOLD) / C5.100/17 | 25. Tria / C5.100/25 | 33. CAPE / C5.100/33 |
| 2. RAKwireless / C5.100/2 | 10. Littelfuse / C5.100/10 | 18. edgebench.io / C5.100/18 | 26. Avnet / C5.100/26 | 34. PICMG / C5.100/34 |
| 3. OPEN / C5.100/3 | 11. ADI (HOLD) / C5.100/11 | 19. ELLi Sales / C5.100/19 | 27. Mender / C5.100/27 | 35. SGeT / C5.100/35 |
| 4. Softeq / C5.100/4 | 12. OPEN / C5.100/12 | 20. OPEN / C5.100/20 | 28. Samtec / C5.100/28 | 36. Renesas / C5.100/36 |
| 5. Digi Int'l / C5.100/5 | 13. DigiKey Pod / C5.100/13 | 21. OPEN / C5.100/21 | 29. Liebherr / C5.100/29 | 37. bytes at work / C5.100/37 |
| 6. OPEN / C5.100/6 | 14. DigiKey Pod / C5.100/14 | 22. ELLi Podcast / C5.100/22 | 30. Aurora Labs(HOLD)C5.100/30 | 38. Schubert / C5.100/38 |
| 7. DigiKey Pod / C5.100/7 | 15. Synaptics / C5.100/15 | 23. Dojo Five / C5.100/23 | 31. congatec / C5.100/31 | 39. Exein / C5.100/39 |
| 8. Weidmuller (Hold) / C5.100/8 | 16. NXP (HOLD) / C5.100/16 | 24. Hackster / C5.100/24 | 32. N-and Group / C5.100/32 | 40. SECO / C5.100/40 |



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NOVEMBER 10-13, 2026
MUNICH, GERMANY

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